CLAIMS

1. A method for generating a modified view of a circuit layout comprising the steps of:

receiving said circuit layout from a design rule clean database;

extracting a base wafer layout from said circuit layout according to a set of computer executable instructions; and

modifying said base wafer layout according to said set of computer executable instructions.

2. The method according to claim 1, wherein the step of extracting said base wafer further comprises:

extracting base layers of one or more unused diffused blocks from said circuit layout.

3. The method according to claim 2, wherein the step of extracting said base wafer further comprises:

extracting layer tags from said circuit layout.

4. The method according to claim 3, wherein the step of modifying said base wafer further comprises:

combining the extracted base layers of said one or more unused diffused blocks into a paveover cell.

5. The method according to claim 4, further comprising:

flattening said paveover cell.

6. The method according to claim 1, further comprising the step of:

comparing one or more base layers of said base wafer with corresponding base layers of said circuit layout.

7. The method according to claim 1, further comprising:

placing routing over said base wafer, wherein said routing uses routing resources of one or more unused diffused blocks.

8. The method according to claim 2, further comprising:

extracting one or more control layers of said one or more diffused blocks.

9. The method according to claim 8, wherein said control layers are extracted based upon any of (i) a clean design rule check (DRC), (ii) a clean layout versus schematic (LVS) check and (iii) both a clean DRC and a clean LVS check.

10. The method according to claim 2, wherein said one or more unused diffused blocks comprise one or more of a hard macro, coreware, a standard cell and a memory.

11. The method according to claim 2, further comprising the steps of:

generating a second design rule clean database comprising said modified view of said circuit layout, wherein said second database is used for subsequent steps of a design when one or more diffused blocks of said circuit layout are unused in said design.

12. A design tool for automating a process for generating a modified view of a circuit layout comprising:

means for extracting base layers of one or more diffused blocks of said circuit layout; and

means for forming a paveover cell comprising the extracted base layers, wherein said design tool facilities reuse or routing resources of said one or more diffused blocks.

13. A design tool for automating a process for generating a modified view of a circuit layout comprising:

a first set of computer executable instructions configured to extract base layers of one or more unused diffused blocks of a circuit layout;

a second set of computer executable instructions configured to generate a paveover cell comprising said extracted base layers; and

a third set of computer executable instructions configured to generate a second database comprising said paveover cell, wherein routing resources of said one or more unused diffused blocks are available for reuse.

14. The design tool according to claim 13, wherein:

said first set of computer executable instructions and said second comprise a run deck configured to control a commercially available tool suite.

15. The design tool according to claim 13, wherein:

said first set of computer executable instructions and said second set of computer executable instructions are stored in a computer readable media.

16. The design tool according to claim 13, further comprising:

a fourth set of computer executable instructions configured to perform one or more operations of inserting metal utilization information (mu), creating route guides, avoiding crosstalk and avoiding slew errors.

17. The design tool according to claim 13, further comprising the step of:

generating a netlist in response to a layout versus schematic (LVS) verification operation on said paveover cell.

18. The design tool according to claim 13, wherein:

said third set of computer executable instructions are further configured to generate said second database according to a

metal utilization (mu) annotation file generated in response to a design rule checking (DRC) operation.

19. The design tool according to claim 13, wherein said design tool is configured to present one or more frame views of said paveover cell.

20. The design tool according to claim 13, further comprising:

a fourth set of computer executable instructions configured to (i) compare one or more base layers of said paveover cell to corresponding base layers of said circuit layout and (ii) assure said base layers of said paveover cell correctly compare with said corresponding base layers of said circuit layout.